REMARKS

In the present Office Action, claims 1-19 were pending before the Office. Of these, claims 1, 11, 16, and 18 were the only independent claims. The Office Action rejected all the claims.

Claim 1 was objected to. Claims 16 - 19 were rejected under 35 U.S.C. §102. Claims 1 - 15 were rejected under 35 U.S.C. §103.

Claim 1 has been amended herein. No claims have been added, canceled, or withdrawn. No new matter has been added by the amendments.

A. CLAIM OBJECTION

Claim 1 was objected to because of informalities. Line 24 of claim 1 has been amended to recite "the control block index." Thus, the Applicants respectfully request withdrawal of the objection.

B. REJECTION OF CLAIMS 16 - 19 UNDER 35 U.S.C. §102

Claims 16 - 19 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,414,701 issued to *Shtayer et al* (hereinafter "*Shtayer*"). For at least the reasons explained below, Applicants respectfully traverse these rejections.

As discussed in more detail below, the Applicants respectfully submit that *Shtayer* fails to teach or suggest every claim feature. For example, *Shtayer* is completely

silent with respect to, for example, “entries stored in a first on-chip memory.”

Claim 16 of the present application recites, inter alia:

> accessing one of a plurality of entries stored in a first on-chip memory using the first index;

and claim 18 recites, inter alia:

> a first on-chip memory having a plurality of entries[.]

Shtayer is directed to performing address compression in an asynchronous transfer mode (ATM) system. In contrast to the above-recited features of the present application, S*htayer* makes no mention whatsoever of an on-chip memory. Rather, *Shtayer* only discusses a link table containing multiple link entries 20a. *Shtayer,* col. 5, lines 33-36. Applicants have reviewed the cited section of *Shtayer* and others and have been unable to find any indication that the link table is stored on an on-chip memory. Thus, *Shtayer* cannot properly be relied upon for teaching or suggesting every feature of independent claims 16 and 18. Accordingly, the Applicants respectfully request that the rejections of claims 16 - 19 be withdrawn.

C. REJECTION OF CLAIMS 1 – 3 AND 5 – 15 UNDER 35 U.S.C. §103

Claims 1 – 3 and 5 – 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Shtayer* in view of U.S. Patent No. 6,356,552 to Foglar (hereinafter "*Foglar*"). For at least the reasons explained below, Applicants respectfully traverse these rejections.

As discussed in more detail below, the Applicants respectfully submit that the proposed combination of *Shtayer* and *Foglar* fails to teach or suggest every claim feature. For example, the Office Action concedes that "*Shtayer* does not disclose expressly… that the first entry specifies a number of bits of the port number to use in the control block index…" *Office Action,* page 5, lines 6 – 7. Further, *Foglar* makes no mention of, for example, "employing the first base memory address and the number of bits of the port number… specified by the first entry to create the control block index for the data cell."

Claim 1 of the present application recites, inter alia:

> employing the first base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the first entry to create the control block index for the data cell[;]

and claim 11 recites, inter alia:

> a logic circuit adapted to:
>
> …
>
> employ the base memory address and the number of bits of the port number, virtual

path identifier and virtual channel identifier specified by the entry to create a control block index for the first data cell.

Foglar is directed to a method by which sets of values representing various parameters can be allocated to addresses, the method being applicable to asynchronous transfer mode (ATM) switching. Applicants understand *Foglar* to use the abbreviation P to refer to pointer. See, e.g., *Foglar*, col. 8, lines 15 - 21. Therefore, in contrast to the above-recited features of the present application, *Foglar* appears to discuss pointer bits with respect to the discussion of FIG. 1 of *Foglar*. Thus, *Foglar* cannot properly be relied upon for teaching or suggesting every feature of independent claims 1 and 11. Accordingly, the Applicants respectfully request that the rejections of claims 1 - 3 and 5 - 15 be withdrawn.

D. REJECTION OF CLAIM 4 UNDER 35 U.S.C. §`103

Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Shtayer* in view of *Foglar* and in further view of U.S. Patent No. 6,272,504 issued to Baentsch et al. (hereinafter *"Baentsch"*). For at least the reasons explained below, Applicants respectfully traverse this rejection.

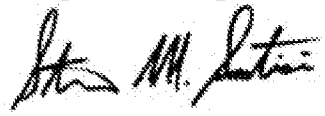
Claim 4 depends ultimately from independent claim 1, the rejection of which is believed to be deficient as discussed above. Applicants have reviewed the cited section of *Baentsch* and others and believe that *Baentsch* fails to make up for the deficiency discussed with respect to the rejection of claim 1. Accordingly, the Applicants respectfully request that the rejection of claim 4 be withdrawn.

E. CONCLUSION

Since the Applicants assert that all the independent claims as amended are in condition for allowance and all remaining claims properly depend from the independent claims, Applicants assert that all claims are allowable.

Applicants do not believe a Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any additional fees are due regarding this Amendment. However, if any additional fees are required, please charge Deposit Account No. 04-1696.

Respectfully Submitted,



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